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10/694,729	10/29/2003	Hoang T. Tran	1875.4520000	4015

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EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
05/29/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,729	TRAN ET AL.	
	Examiner	Art Unit	
	SCOTT SUN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/18/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/18/2009 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

   a. Prior art of record do not teach a bus coupling the parallel and serial ports. Specifically, the parallel and serial ports of prior art appear to be independent and not interconnected.

2. Regarding argument 'a', examiner notes that prior art of record, Weber, shows in figure 4 that the various serializers and deserializers are interconnected. There are various other processing elements in between the connections (encoders, decoders, data presenters, buffers, protocol processors, etc...), but the serializers and deserializers are still coupled at the end of these connections. This is further evidenced by the fact Weber teaches (paragraphs 23-25) that data is received by one of the SERDES circuits 410-413 and, after processing through the intermediate elements, again transmitted by the SERDES circuits 410-413. Clearly, these SERDES circuits 410-413 are interconnected, or otherwise the data would not be received by any one of these circuits and then subsequently transmitted by any one of these circuits.

3. Having responded to each of applicant's arguments, examiner notes that prior art of record still provides a valid ground of rejection, as attached below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 15, 16, 18-20, 25-27, and 31-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber et al (previously cited) in view of Kim et al (Pub #2002/0163924, hereinafter Kim).

6. Regarding claim 12, Weber discloses a transceiver (system 400 in figure 4), comprising: a plurality of ports, wherein said plurality of ports includes at least one parallel port and at least one serial port (serializer/deserializers 410-413 functioning in serial or parallel for STMS or MTSS protocol, figure 4, paragraph 18 and 25);

a bus (connections between the various elements in figure 4) coupled to said plurality of ports on a common substrate (single die, line 8, paragraph 22) wherein said bus is configured to couple at least one of said first parallel port to at least one of a second parallel port and to said first serial port and said first serial port to at least one of a second serial port and said first parallel port (all SERDES are interconnected as shown in figure 4);

Weber does not disclose explicitly a plurality of programmable pads in the parallel/serial ports. However, Kim discloses a plurality of programmable pads (GPIO, general purpose input-output), and wherein at least one of said first programmable pad

and said second programmable pad is configurable to operate according to a plurality of electrical specifications and a plurality of data protocols (configuring the general purpose input output port to the specification of the attached device, paragraphs 24, 27)

A pad control system (configuration register, paragraph 24, example shown in figure 2) to configure said at least one of said first programmable pad and said second programmable pad to operate in accordance with a specified data protocol of said plurality of data protocols and a specified electrical specification of said plurality of electrical specifications (various protocols and electric specifications in paragraph 27, although other protocols and electrical specifications would have been obvious given the teachings of GPIO)

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Weber and Kim by using GPIOs in the system of Weber for the benefit of reducing the number of I/O pins needed (paragraph 3, Kim).

7. Regarding claim 15, Weber and Kim combined disclose claim 12 and Weber further discloses an input controller (protocol processors 450-455) to configure said least one of said programmable pad and said second programmable pad to receive at least one of a data signal and a control signal (lines 6-11, paragraph 16, lines 1-9, paragraph 23).

8. Regarding claim 16, Weber and Kim combined disclose claim 12 and Weber further discloses an output controller (protocol processors 450-455) to configure said least one of said programmable pad and said second programmable pad to send at

least one of a data signal and a control signal (lines 1-6, paragraph 17, 1-11, paragraph 24).

9. Regarding claims 18-20 and 25-27, examiner notes that these claims contain limitations substantially similar to those in claims 12, 15 and 16. The same grounds of rejection are applied.

10. Regarding claims 31, 33, and 36, examiner notes that Weber discloses using 10 Gb Ethernet as an exemplary embodiment. Other 10 Gb protocols would be obvious design choices given the teachings of Weber (paragraph 28).

11. Regarding claim 32, Weber and Kim combined disclose claim 12, and Weber further discloses wherein said first parallel port is configured to operate at 1/10 of a data rate of said first serial port (paragraph 23). Examiner notes that Weber discloses serial data are converted to lower speed parallel data, and one of ordinary skill would readily recognize that 10 bit coding parallel data are 1/10 of the speed of its serial counterpart.

12. Regarding claim 34, Weber and Kim combined disclose claim 12, and Weber further discloses at least one serial port is configured to operate at a plurality of data rates (paragraph 14).

13. Regarding claim 35, Weber and Kim combined disclose claim 34, and examiner notes that the data rates are obvious design choices given the teachings of Weber to have variable rates of data transfer (paragraph 26).

14. Regarding claim 37 and 38, Weber and Kim combined disclose claim 12, and Weber further discloses serial/parallel conversion (serializers and deserializers in figure 4).

15. Regarding claim 39, Weber and Kim combined disclose claim 12, and Kim further discloses a register (configuration register, paragraph 24) for sending instructions to configure said at least one of said first programmable pad and said second programmable pad to comply with said specified data protocol and said specified electrical specification (paragraph 27).

16. Regarding claim 40, Weber and Kim combined disclose claim 12, and Kim further discloses wherein an operating voltage of said at least one of said first programmable pad and said second programmable pad is changed according to said specified eletrical specification (paragraph 27).

17. Regarding claim 41, Weber and Kim combined disclose claim 12, and Kim further discloses wherein said at least one of said first programmable pad and aid second programmable pad is configured to either send or receive data after having been configured to comply with said specified data protocol and said specified electrical specification (output/input enable register entries, paragraph 25)

18. Regarding claims 42-49, examiner notes that these claims are substantially similar to claims 39-41 above. The same grounds of rejection are applied.

19. Claims 17, 21, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Kim and further in view of Rearick et al (previously cited).

20. Regarding claim 17, Weber and Kim combined disclose claim 12 but do not disclose explicitly measuring leakage current. However, Rearick discloses a testing register (driver test system 200, figure 2) configured to send a test message to measure leakage current (tri-state leakage current) from said at least one of first programmable pad and said second programmable pad (paragraphs 33, 40). Teachings of Weber, Kim and Rearick are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Kim and Rearick by adding Rearick's testing circuit to the combined system of Weber and Kim for the benefit of providing cost-effective and accurate self-testing capability to the integrated circuit (background, Rearick).

21. Regarding claims 21 and 28, examiner notes that these claims contain limitations substantially similar to those in claim 17. The same grounds of rejection are applied.

22. Claims 13, 14, 22-24, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber in view of Kim and further in view of Taniguchi et al (previously cited).

23. Regarding claim 13, Weber and Kim combined disclose claim 12 but do not disclose explicitly adjusting a delay between input and output. However, Taniguchi discloses a timing controller (delay adjustment circuit, figure 5) configured to modulate delay between an input (input of buffer) and an output (output of buffer) of an integrated

circuit (DLL Array 7; paragraphs 52, 53). Teachings of Weber, Kim and Taniguchi are from the same field of integrated circuits.

Therefore, it would have been obvious at the time of invention to combine teachings of Weber, Kim and Taniguchi by using the adjustable delay circuit disclosed by Taniguchi in the combined system of Weber and Kim for the benefit of underflow and overflow prevention (paragraph 87, Taniguchi).

24. Regarding claim 14, Weber and Kim combined disclose claim 12, and Taniguchi further discloses a timing register configured to send instructions to adjust the delay between input and output of at least one of said programmable pads. Examiner notes that the same reasons to combine the teachings of Weber and Taniguchi can be applied. Examiner further notes that Kim also briefly discusses a timing register (interrupt register, paragraph 26)

25. Regarding claims 22-24 and 29-30, examiner notes that these claims contain limitations substantially similar to those in claim 13 and 14 above. The same grounds of rejection are applied. Further regarding claims 23 and 24, Examiner notes that Taniguchi discloses that the data is delayed in a buffer (input/output buffer), where the delay is a fixed time interval set by the delay adjustor circuit (figure 5, paragraphs 9, 52).

Examiner Comment

26. The following subject matter drafted by the examiner and considered to distinguish patentably over the art of record in this application, is presented to applicant for consideration:

The bus forms a ring structure around a center logic core and connects the plurality of ports on the common substrate in a rotational symmetric layout such that the transceiver maintains its functionality and configuration when rotated.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SCOTT SUN whose telephone number is (571)272-2675. The examiner can normally be reached on Mon-Thu, 10:00am-8pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182